IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Wendell P. Noble et al.	Examiner: Jack Chen
Serial No.:	09/866,938	Group Art Unit: 2813
Filed:	May 29, 2001	Docket: 303.330US3
Title:	ULTRA HIGH DENSITY FLASH MEMORY	

COMMUNICATION CONCERNING CO-PENDING APPLICATION(S)

Commissioner for Patents
Washington, D.C. 20231

Applicant would like to bring to the Examiner's attention the following related co-pending application(s) in the above-identified patent application:

Serial No.	Filing Date	Attorney Docket	Title
09/527,981	03/17/2000	00303.322US2	FOUR F2 FOLDED BIT LINE DRAM CELL STRUCTURE HAVING BURIED BIT AND WORD LINES
09/571,352	05/16/2000	00303.322US3	FOUR F2 FOLDED BIT LINE DRAM CELL STRUCTURE HAVING BURIED BIT AND WORD LINES
09/510,095	02/22/2000	00303.323US2	SEMICONDUCTOR-ON-INSULATOR MEMORY CELL WITH BURIED WORD AND BODY LINES
09/139,164	08/24/1998	00303.328US2	MEMORY CELL HAVING A VERTICAL TRANSISTOR WITH BURIED SOURCE/DRAIN AND DUAL GATES
09/596,266	06/16/2000	00303.328US3	MEMORY CELL HAVING A VERTICAL TRANSISTOR WITH BURIED SOURCE/DRAIN AND DUAL GATES
09/651,199	08/30/2000	00303.328US4	MEMORY CELL HAVING A VERTICAL TRANSISTOR WITH BURIED SOURCE/DRAIN AND DUAL GATES
09/789,274	02/20/2001	00303.329US4	MEMORY CELL WITH VERTICAL TRANSISTOR AND BURIED WORD AND BODY LINES

09/551,027	04/17/2000	00303.379US2	CIRCUIT AND METHOD FOR A FOLDED BIT LINE MEMORY CELL WITH VERTICAL TRANSISTOR AND TRENCH CAPACITOR
08/944,890	10/06/1997	00303.380US1	CIRCUIT AND METHOD FOR AN OPEN BIT LINE MEMORY CELL WITH A VERTICAL TRANSISTOR AND TRENCH PLATE TRENCH CAPACITOR
09/730,245	12/05/2000	00303.380US3	CIRCUIT AND METHOD FOR AN OPEN BIT LINE MEMORY CELL WITH A VERTICAL TRANSISTOR AND TRENCH PLATE TRENCH CAPACITOR
09/467,992	12/20/1999	00303.389US2	CIRCUITS WITH A TRENCH CAPACITOR HAVING MICRO-ROUGHENED SEMICONDUCTOR SURFACES
09/742,568	12/20/2000	00303.393US3	CIRCUIT AND METHOD FOR AN OPEN BIT LINE MEMORY CELL WITH A VERTICAL TRANSISTOR AND TRENCH PLATE TRENCH CAPACITOR
09/669,281	09/26/2000	00303.405US3	PROGRAMMABLE MEMORY ADDRESS DECODE ARRAYS WITH VERTICAL TRANSISTOR
09/520,494	03/08/2000	00303.406US2	FIELD PROGRAMMABLE LOGIC ARRAYS WITH VERTICAL TRANSISTORS
09/756,089	01/08/2001	00303.407US2	PROGRAMMABLE LOGIC ARRAY WITH VERTICAL TRANSISTORS
09/756,099	01/08/2001	00303.407US3	PROGRAMMABLE LOGIC ARRAY WITH VERTICAL TRANSISTORS
09/650,600	08/30/2000	00303.408US2	MEMORY ADDRESS DECODE ARRAY WITH VERTICAL TRANSISTORS

09/879,592	06/12/2001	00303.412US2	VERTICAL GAIN CELL AND ARRAY FOR A DYNAMIC RANDOM ACCESS MEMORY AND METHOD FOR FORMING THE SAME
09/879,602	06/12/2001	00303.412US3	VERTICAL GAIN CELL AND ARRAY FOR A DYNAMIC RANDOM ACCESS MEMORY AND METHOD FOR FORMING THE SAME
09/498,433	02/04/2000	00303.464US2	CIRCUITS AND METHODS FOR A MEMORY CELL WITH A TRENCH PLATE TRENCH CAPACITOR AND A VERTICAL BIPOLAR READ DEVICE

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 7 day of May, 2002.

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